ABSTRACT OF THE DISCLOSURE

An architecture for testing a plurality of circuits on an integrated circuit is described. The architecture includes a TAP Linking Module located between test pins on the integrated circuit and 1149.1 Test Access Ports (TAP) of the plurality of circuits to be tested. The TAP Linking Module operates in response to 1149.1 scan operations from a tester connected to the test pins to selectively switch between 1149.1 TAPs to enable test access between the tester and plurality of circuits. The TAP Linking Module's 1149.1 TAP switching operation is based upon augmenting 1149.1 instruction patterns to affix an additional bit or bits of information which is used by the TAP Linking Module for performing the TAP switching operation.